Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	869	(trench with (tapering or tapered))	US-PGPUB; USPAT	OR	ON	2005/03/02 15:27
L4	819	3 and @ad<"20031031"	US-PGPUB; USPAT	OR	ON	2005/03/02 15:15
L5	249	4 and RIE	US-PGPUB; USPAT	OR	ON	2005/03/02 15:27
L6	252	(trench with (tapering or tapered))	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/02 15:27
L7	13	6 and RIE	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/02 15:28

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1841	((tapered or tapering or rounding or rounded) with trench)	US-PGPUB; USPAT	OR	ON	2005/03/02 17:48
L2	1716	1 and @ad<"20031031"	US-PGPUB; USPAT	OR	ON	2005/03/02 17:48
L3	368	2 and (trench with (lining or liner or adhesion or adhesive))	US-PGPUB; USPAT	OR	ON	2005/03/02 17:49
L4	121	3 and ((lining or liner or adhesion or adhesive) with (depositing or deposition))	US-PGPUB; USPAT	OR	ON	2005/03/02 17:49

DOCUMENT-IDENTIFIER: US 20040198038 A1

TITLE: METHOD OF FORMING SHALLOW TRENCH ISOLATION WITH
CHAMFERED CORNERS

---------- KWIC ---------

Abstract Paragraph - ABTX (1):

A method of forming shallow trench isolation with chamfered corners. First, a pad insulating layer, a first mask layer, and a second mask layer are sequentially formed on a substrate. The second mask layer, the first mask layer, and the pad insulating layer are patterned to form an opening exposing a portion of the substrate. Next, the substrate is etched using the patterned second mask layer as a mask to form a trench therein. Next, part of the second mask layer is removed to expose, the first mask layer adjacent to the **trench** and result in the second mask layer having a **tapered** profile. Finally, the second mask layer, the first mask layer, the pad insulating layer, and the substrate are etched along the **tapered** profile of the second mask layer to chamfer corners of the **trench**.

Summary of Invention Paragraph - BSTX (19):

[0017] To achieve the above mentioned objects, the method of forming shallow trench isolation with chamfered corners according to the present invention includes the following steps. First, a pad insulating layer, a first mask layer, and a second mask layer are sequentially formed on a substrate. The second mask layer, the first mask layer, and the pad insulating layer are patterned to form an opening exposing a portion of the substrate. Next, the substrate is etched using the patterned second mask layer as a mask to form a trench therein. Next, part of the second mask layer is removed to expose the first mask layer adjacent to the **trench** and result in the second mask layer having a **tapered** profile. Finally, the second mask layer, the first mask layer, the pad insulating layer, and the substrate are etched along the **tapered** profile of the second mask layer to chamfer corners of the **trench**.

Summary of Invention Paragraph - BSTX (23):

[0021] The present invention also provides another method of forming shallow trench isolation with chamfered corners, including the following steps. First, a pad insulating layer, a first mask layer, and a second mask layer are sequentially formed on a semiconductor substrate. Then, the second mask layer,

the first mask layer, and the pad insulating layer are patterned to form an opening exposing a portion of the semiconductor substrate. Next, the semiconductor substrate is etched using the patterned second mask layer as a mask to form a trench therein. Next, part of the second mask layer is removed to expose the first mask layer adjacent to the **trench** and result in the second mask layer having a **tapered** profile. Next, the second mask layer, the first mask layer, the pad insulating layer, and the substrate are etched along the **tapered** profile of the second mask layer to chamfer corners of the **trench**. Furthermore, the second mask layer is completely removed. A shield layer is formed on the surface of the substrate, the trench, and the chamfered corners. An insulator layer is blanketly formed on the shield layer to fill the trench. Finally, the first mask layer and the pad insulating layer are removed to form the trench isolation region.

Detail Description Paragraph - DETX (9):

[0036] Subsequently, referring to FIG. 4D, anisotropic etching, for example **RIE,** is performed along the **tapered** profiles 108 of the second mask layer 106 to remove part of the second mask layer 106, the first mask layer 104, the pad insulating layer 102, and the semiconductor substrate 100 around the **trenches** 105. Then, the corners 110 of the trench 105 are chamfered, and a Y-shaped trench 105a is further formed. The depth 120a (for example, between 2700.about.3600 .ANG.) of the Y-shaped trench 105a is deeper than that of the original trench 105, and the aspect ratio of the Y-shaped trench is between 4.about.6.

Claims Text - CLTX (2):

1. A method of forming shallow trench isolation with chamfered corners, comprising: forming a pad insulating layer, a first mask layer, and a second mask layer on a substrate; patterning the second mask layer, the first mask layer, and the pad insulating layer to form an opening exposing a portion of the substrate; etching the substrate using the patterned second mask layer as a mask to form a trench in the substrate; removing part of the second mask layer to expose the first mask layer adjacent to the **trench** and result in the second mask layer having a **tapered** profile; and etching the second mask layer, the first mask layer, the pad insulating layer, and the substrate along the **tapered** profile of the second mask layer to chamfer corners of the **trench**.

Claims Text - CLTX (15):

14. A method of forming shallow trench isolation with chamfered corners, comprising: forming a pad oxide layer, a first mask layer, and a second mask layer on a substrate; patterning the second mask layer, the first mask layer, and the pad oxide layer to form an opening exposing a portion of the substrate;

etching the substrate using the patterned second mask layer as a mask to form a trench in the substrate; removing part of the second mask layer by wet etching to expose the first mask layer adjacent to the **trench** and result in the second mask layer having a **tapered** profile; etching the second mask layer, the first mask layer, the pad insulating layer, and the substrate along the **tapered** profile of the second mask layer to chamfer corners of the **trench**; completely removing the second mask layer; forming a liner oxide layer on the surface of the substrate, the trench, and the chamfered corners, blanketly forming aN insulator layer on the exposed surface of the substrate and the chamfered corners thereof to fill the trench; and flattening the insulator layer, and removing the first mask layer and the pad oxide layer to form a trench isolation region.

DOCUMENT-IDENTIFIER: US 20040102005 A1

TITLE: Method of manufacturing a semiconductor device

---------- KWIC ---------

Detail Description Paragraph - DETX (8):

[0021] Referring to FIG. 1B, the pad nitride film 16, the first polysilicon film 14, the tunnel oxide film 12 and the semiconductor substrate 10 are sequentially etched through an ISO (isolation) mask patterning to form a trench 18 of a STI (shallow trench isolation) structure, thus defining an active region and a field region. A dry oxidization process for compensating for etch damage at the sidewall of the **trench** 18 of the STI structure is implemented to make **rounded** the corner of the **trench** 18. High temperature oxide (HTO) is thinly deposited on the entire structure and is then experienced by a densification process at high temperature, thus forming a liner oxide film (not shown). At this time, in order to simplify the process, the process of **depositing the liner** oxide film may be omitted.

Detail Description Paragraph - DETX (9):

[0022] In detail, after a photoresist film is covered on the entire structure, a photolithography process using the photoresist film as a mask is implemented to form a photoresist film pattern (not shown). An etch process using the photoresist film pattern as an etch mask is then implemented to etch the pad nitride film 16, the first polysilicon film 14, the tunnel oxide film 12 and the semiconductor substrate 10, thus forming the trench 18 of the STI structure. In forming the trench, the semiconductor substrate is etched to have a specific tilt angle of 65.about.85.degree.. In order to compensate for damage of the sidewall of the **trench** 18 due to the etch process and make **rounded** the top corner of the **trench,** a dry oxidization process is implemented at a temperature of 750.about.900.degree. C. to form an oxide film 20 of 50.about.150 .ANG. in thickness. A low dry oxidization process is implemented to minimize diffusion of the ions implanted in order to control the well or the threshold voltage (Vt), so that a normal junction and well are kept.

Detail Description Paragraph - DETX (10):

[0023] In order to improve an **adhesive** characteristic between an oxide film in a subsequent process and the **trench** 18 and prevent generation of a moat, HTO formed using DCS (dichloro silane; SiH.sub.2CL.sub.2) gas is deposited in thickness of 50.about.150 .ANG.. A high temperature densification process is

then implemented using N.sub.2 at a temperature of 1000.about.1100.degree. C. for 20.about.30 minutes, thus forming a liner oxide film (not shown). As the tissue of liner oxide film is made dense by the high temperature densification process, it helps to increase the etch resistance, prohibit formation of a moat when implementing STI and prevent the leakage current.